WE CLAIM:

1. A method for controlling a dual-slope integrator circuit, the integrator circuit having an integrating capacitor, a reset input for receiving a reset signal that is used in maintaining a reset state of the integrating capacitor, and an integrator input for receiving a signal to be integrated, said method comprising the steps of:

a) in response to an original input signal, generating the reset signal that is provided to the reset input and that has a predetermined reset time period;

b) simultaneous with step a), generating a delayed input signal by introducing a predetermined delay period into the original input signal, the delay period being longer than the reset time period; and

c) with reference to the original input signal and the delayed input signal, generating a trigger signal that is provided to the integrator input for enabling charging operation of the integrating capacitor during a charging period that starts from the end of the reset time period and that terminates at a lagging edge of the delayed input signal.

2. The method as claimed in Claim 1, wherein the original input signal is a pulse signal.

3. The method as claimed in Claim 1, wherein the charging period includes a pre-charging sub-period that starts from the end of the reset time period and that terminates

at a leading edge of the delayed input signal, and an actual integrating sub-period that follows the pre-charging sub-period and that has a duration equal to that of the original input signal.

4. The method as claimed in Claim 3, wherein the pre-charging sub-period is longer than a measured settling time of the integrator circuit.

5. A method for controlling a dual-slope integrator circuit, the integrator circuit having an integrating capacitor, a reset input for receiving a reset signal that is used in maintaining a reset state of the integrating capacitor, and an integrator input for receiving a signal to be integrated, said method comprising the steps of:

a) in response to an original input signal, generating a trigger signal that is provided to the integrator input;

b) simultaneous with step a), generating the reset signal that is provided to the reset input and that has a predetermined reset time period such that charging operation of the integrating capacitor is enabled only at the end of the reset time period;

c) simultaneous with step a), generating a delayed input signal by introducing a predetermined delay period into the original input signal, the delay period being longer than the reset time period; and

d) terminating generation of the trigger signal upon detection of a lagging edge of the delayed input signal.

6. The method as claimed in Claim 5, wherein the original input signal is a pulse signal.

7. The method as claimed in Claim 5, wherein the delay period is longer than the reset time period by a duration not smaller than a measured settling time of the integrator circuit.

8. An apparatus for controlling a dual-slope integrator circuit, the integrator circuit having an integrating capacitor, a reset input for receiving a reset signal that is used in maintaining a reset state of the integrating capacitor, and an integrator input for receiving a signal to be integrated, said apparatus comprising:

a one-shot circuit adapted to receive an original input signal and to generate the reset signal, that is provided to the reset input and that has a predetermined reset time period, in response to the original input signal;

a delay circuit adapted to receive the original input signal and to generate a delayed input signal by introducing a predetermined delay period into the original input signal, the delay period being longer than the reset time period; and

a control circuit adapted to receive the original input signal and the delayed input signal and to generate a trigger signal that is provided to the integrator input for enabling charging operation of the integrating

capacitor during a charging period that starts from the end of the reset time period and that terminates at a lagging edge of the delayed input signal.

9. The apparatus as claimed in Claim 8, wherein said control circuit generates the trigger signal starting from a leading edge of the original input signal and terminating at the lagging edge of the delayed input signal.

10. The apparatus as claimed in Claim 8, wherein said control circuit includes:

a latch having a first input terminal for receiving the original input signal, a second input terminal for receiving the delayed input signal, and an output terminal; and

a logic gate having a first input terminal for receiving the delayed input signal, a second input terminal coupled to said output terminal of said latch, and an output terminal from which the trigger signal is obtained.

11. The apparatus as claimed in Claim 10, wherein said latch is an SR latch having a set terminal that serves as said first input terminal and a reset terminal that serves as said second input terminal, and said logic gate is a logic NOR gate.

12. The apparatus as claimed in Claim 8, wherein the charging period includes a pre-charging sub-period that starts from the end of the reset time period and that

terminates at a leading edge of the delayed input signal, and an actual integrating sub-period that follows the pre-charging sub-period and that has a duration equal to that of the original input signal.

13. The apparatus as claimed in Claim 12, wherein the pre-charging sub-period is longer than a measured settling time of the integrator circuit.

14. An apparatus for controlling a dual-slope integrator circuit, the integrator circuit having an integrating capacitor, a reset input for receiving a reset signal that is used in maintaining a reset state of the integrating capacitor, and an integrator input for receiving a signal to be integrated, said apparatus comprising:

a control circuit adapted to receive an original input signal and to generate a trigger signal, that is provided to the integrator input, in response to the original input signal;

a one-shot circuit adapted to receive the original input signal and to generate the reset signal, that is provided to the reset input and that has a predetermined reset time period, in response to the original input signal;

charging operation of the integrating capacitor being enabled by said one-shot circuit only at the end of the reset time period; and

a delay circuit adapted to receive the original input signal and to generate a delayed input signal by introducing a predetermined delay period into the original input signal, the delay period being longer than the reset time period;

said control circuit being coupled to said delay circuit so as to receive the delayed input signal therefrom, and terminating generation of the trigger signal upon detection of a lagging edge of the delayed input signal.

15. The apparatus as claimed in Claim 14, wherein said control circuit generates the trigger signal starting from a leading edge of the original input signal and terminating at the lagging edge of the delayed input signal.

16. The apparatus as claimed in Claim 14, wherein said control circuit includes:

a latch having a first input terminal for receiving the original input signal, a second input terminal for receiving the delayed input signal, and an output terminal; and

a logic gate having a first input terminal for receiving the delayed input signal, a second input terminal coupled to said output terminal of said latch, and an output terminal from which the trigger signal is obtained.

17. The apparatus as claimed in Claim 16, wherein said latch is an SR latch having a set terminal that serves as said first input terminal and a reset terminal that serves as said second input terminal, and said logic gate is a logic NOR gate.

18. The method as claimed in Claim 14, wherein the delay period is longer than the reset time period by a duration not smaller than a measured settling time of the integrator circuit.